REMARKS

Claims 1 to 14 are now pending and being considered.

It is respectfully submitted that all of the presently pending claims are allowable, and reconsideration is respectfully requested.

With respect to paragraph six (6) of the Final Office Action, claims 1 to 9 were rejected as non-statutory under Section 101.

Applicants do not understand why the Examiner is raising this issue for the first time. To the extent that the Examiner maintains this rejection, it is respectfully requested that the Examiner withdraw the finality of the Office Action since the prior response did not result in this rejection. Still further, it is respectfully submitted that claim 1 does satisfy Section 101 since it is directed to a process which is patentable and since it has utility. It is suggested that the Examiner read the MPEP at 2106 and 2107 regarding the Examination Guidelines for the utility requirement.

It is also respectfully submitted that the reasons advanced in support of the rejection are simply not supported by either the Examination Guidelines or the case law, and that a prima facie case has not been presented as required by Sections 2106 and 2107 of the MPEP.

In this regard, the Board of Patent Appeals — in reversing another Examiner for ignoring the law of State Street — has stated that claimed subject matter having a "practical application" is § 101 statutory subject matter if it represents a "useful, concrete and tangible result" under State Street, and has further stated that the Federal Circuit's reasoning in State Street is "intended to be broadly construed". See Ex parte Donner, 53 U.S.P.Q.2d 1699, 1702 (Bd. Pat. App. & Int. 1999).

Still further, the Federal Circuit -- as well as the Patent Office — has not required that method claims recite how the method steps are to be performed. In AT&T Corp. v. Excel Communications Inc., 50 U.S.P.Q.2d 1447 (Fed. Cir. 1999), the Federal Circuit stated that the claims of U.S. Patent No. 5,333,184 ("the '184 patent") were plainly directed to § 101 statutory subject matter. See id. at 1452. ("Excel also contends that because the process claims at issue lack physical limitations set forth in the patent, the claims are not patentable subject matter. This argument reflects a misunderstanding of our case law. . . . Since the claims at issue in this case are directed to a process in the first instance, a structural inquiry is unnecessary").

Nevertheless, to facilitate matters, claim 1 has been rewritten to recite a program on a computer medium that is executable on the at least one microprocessor.

It is therefore respectfully requested that the Section 101 rejections be withdrawn as to claims 1 to 9.

With respect to paragraph eight (8), claims 1 to 4, 7, 8, and 10 to 14 were rejected under 35 U.S.C. § 103(a) as unpatentable over the purported "admitted prior art" in view of U.S. Patent No. 6,502,209 ("Bengtsson"), and in further view of Hollander et al., U.S. Patent No. 6,412,071.

In rejecting a claim under 35 U.S.C. § 103(a), the Examiner bears the initial burden of presenting a prima facie case of obviousness. In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). To establish prima facie obviousness, three criteria must be satisfied. First, there must be some suggestion or motivation to modify or combine reference teachings. In re Fine, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). This teaching or suggestion to make the claimed combination must be found in the prior art and not based on the application disclosure. In re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Second, there must be a reasonable expectation of success. In re Merck & Co., Inc., 800 F.2d 1091, 231 U.S.P.Q. 375 (Fed. Cir. 1986). Third, the prior art reference(s) must teach or suggest all of the claim features. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974).

The "Bengtsson" reference refers to the development of a debug-supplement to provide for the possibility to debug systems with a cache memory. This is the normal usage of a debug hardware in the real and concrete meaning of the word debugging.

In contrast, the claimed subject matter concerns the usage of an already existing debug functionality of the microcomputer to realize a monitoring of the stack memory. With this background a secure monitoring of the microcomputer is possible without absorbing run-time and resources of the CPU. So the presently claimed subject matter does not describe the conception, design or development of a debug logic for a microcomputer, but the usage of this for debugging normally used hardware in the software of the microcomputer itself when the microcomputer is in operation and not in debug mode. This is described in the specification on page 5, line 10 to line 17 and from line 19 to 23 on the same page and also on page 10, line 23 to page 11, line 10. This difference is also valid for the Figures 2 and 3 of the present application.

The third-level "Hollander" reference does not describe such a usage of debugging hardware or debug logic.

Still further, claims 1, 10, and 13, as presented, provide for monitoring *an execution of a program* that is executable on at least one microprocessor of a micro controller using a debug logic of the micro controller such that the *debug logic triggers an exception upon access to a specific address range during a program execution time,* the at least one microprocessor configures the debug logic, and the debug logic executes an exception routine *after the exception is triggered during the program execution time.* Furthermore, claims 1, 10, and 13 provide that the access to the specific address range includes *illegal access to a storage area.*

In contrast, the background information discussed in specification states that "[i]n the methods known from the related art, only legal accesses to the I/O ports are handled. In the framework of the known methods, the commands and/or the program are not monitored for possible faults. The known method therefore simply involves an expansion of the operating system." (See Specification, page 4, lines 6 to 9).

Accordingly, this does not disclose or even suggest the feature of a debug logic triggering an exception upon access to a specific address range during a program execution time and executing an exception routine after the exception is triggered during the program execution time such that the access to the specific address range includes illegal access to a storage area. The background information merely indicates that only legal accesses to the I/O ports are handled such that commands and/or programs are not monitored for possible faults. Nothing in the background information discloses (or suggests) the features a debug logic triggering an exception upon access to a specific address range during a program execution time and executing an exception routine after the exception is triggered during the program execution time such that the access to the specific address range includes illegal access to a storage area, as provided for in the context of claims 1, 10, and 13, as presented.

Additionally, the Office Action asserts that while the "[a]dmitted prior art does not explicitly disclose causing the at least one microprocessor to configure the debug logic", the "Bengtsson" reference "discloses in an analogous computer system the debug chip is configured in DUT (device under test)". (Office Action, page 4).

The "Bengtsson" reference concerns "a computer chip having integrated thereon a CPU and a cache system being interconnected, and at least one synchronization unit, said chip being setable in either one of at least two different running modes, a first one thereof being a device under test (DUT) mode, and a second one thereof being a MONITOR mode" and "[t]he chip further comprises a debug bus connectable to another identical chip for

communicating signals enabling the chip and said another chip to run in parallel while said chips are set in complementary modes." (Col. 2, lines 32 to 43). Furthermore, the "Bengtsson" reference states that a "computer system 98 includes a chip 110C in DUT mode" and "[t]he monitor 100 includes two chips with enhanced debug capability 110A-B configured in MONITOR mode." (Col. 3, lines 54 to 65).

The "Bengtsson" reference further states that "a debug bus 140 is coupled to all chips 110A-C for synchronizing their activity including: power-on-reset, interrupts, wait states, DMA accesses and other asynchronous events" and that "only the debug chip 110C configured in DUT mode has its address line coupled to the address portion 146 of the system bus 146-148" such that debug chip 110C "acts as the master of the address portion of the system bus" and "determines what access requests will be handled on the address bus and therefore what data and or program code will be present on the data portion 148 of the system bus." Also, the "Bengtsson" references states that "[a] typical program sequence provided over the data portion of the system bus to each of the chips 110A-C might include a read or write instruction to a specific address followed by data being read from or written to that specific address by each of the above-mentioned chips" and that "[e]ach of the MONITOR mode chips 110A-B therefore shadows the activity of the master chip 110C receiving identical data and instructions and performing the same operations 170C in response, for example, to the program code 180 stored in main memory" such that "[n]one of the monitor chips write to external memory 114" and "[t]he external memory is always written to only by the DUT mode debug chip 110C." (Col. 4, lines 21 to 56).

Accordingly, the "Bengtsson" reference does not disclose or even suggest the feature of a debug logic triggering an exception upon access to a specific address range during a program execution time and executing an exception routine after the exception is triggered during the program execution time such that the access to the specific address range includes illegal access to a storage area. The "Bengtsson" reference merely indicates that a debug chip is the master of an address portion of a system bus and it determines what access requests will be handled on the address bus and what data and/or program code will be present on a data portion of the system bus. Nothing in the "Bengtsson" reference discloses or suggests the feature of a debug logic triggering an exception upon access to a specific address range during a program execution time and executing an exception routine after the exception is triggered during the program execution time such that the access to the specific address range

includes illegal access to a storage area, as provided for in the context of claims 1, 10, and 13, as presented.

Furthermore, the Office Action conclusorily asserts that "it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of configuring the microprocessor or DUT to debug logic as taught by Bengtsson in to the method of monitoring the program as taught in admitted prior art." (Office Action, pages 4).

It is respectfully submitted that the cases of In re Fine, supra, and In re Jones, 21 U.S.P.Q.2d 1941 (Fed. Cir. 1992), make plain that the Office Action's generalized assertions that it would have been obvious to modify or combine the references do not properly support a § 103 rejection. It is respectfully submitted that those cases make plain that the Office Action reflects a subjective "obvious to try" standard, and therefore does not reflect the proper evidence to support an obviousness rejection based on the references relied upon. In particular, the Court in the case of In re Fine stated that:

> The PTO has the burden under section 103 to establish a *prima facie* case of obviousness. It can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. This it has not done. . . .
>
> **Instead, the Examiner relies on hindsight in reaching his obviousness determination. . . . One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.**

In re Fine, 5 U.S.P.Q.2d at 1598 to 1600 (citations omitted; italics in original; emphasis added). Likewise, the Court in the case of In re Jones stated that:

> Before the PTO may combine the disclosures of two or more prior art references in order to establish *prima facie* obviousness, there must be some suggestion for doing so, found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. . . .
>
> **Conspicuously missing from this record is any evidence, other than the PTO's speculation (if it be called evidence) that one of ordinary skill . . . would have been motivated to make the modifications . . . necessary to arrive at the claimed [invention].**

In re Jones, 21 U.S.P.Q.2d at 1943, 1944 (citations omitted; italics in original).

That is exactly the case here since it is believed and respectfully submitted that the present Office Action offers no evidence whatsoever, but only conclusory hindsight, reconstruction and speculation, which these cases have indicated does not constitute evidence that will support a proper obviousness finding. Unsupported assertions are not evidence as to why a person having ordinary skill in the art would be motivated to modify or combine references to provide the claimed subject matter of the claims to address the problems met thereby. Accordingly, the Office must provide proper evidence of a motivation for modifying or combining the references to provide the claimed subject matter.

More recently, the Federal Circuit in the case of In re Kotzab has made plain that even if a claim concerns a "technologically simple concept" — which is not the case here — there still must be some finding as to the "specific understanding or principle within the knowledge of a skilled artisan" that would motivate a person having no knowledge of the claimed subject matter to "make the combination in the manner claimed," stating that:

> In this case, the Examiner and the Board fell into the hindsight trap. The idea of a single sensor controlling multiple valves, as opposed to multiple sensors controlling multiple valves, is a technologically simple concept. With this simple concept in mind, the Patent and Trademark Office found prior art statements that in the abstract appeared to suggest the claimed limitation. But, there was no finding as to the specific understanding or principle within the knowledge of a skilled artisan that would have motivated one with no knowledge of Kotzab's invention to make the combination in the manner claimed. In light of our holding of the absence of a motivation to combine the teachings in Evans, we conclude that the Board did not make out a proper prima facie case of obviousness in rejecting [the] claims . . . under 35 U.S.C. Section 103(a) over Evans.

In re Kotzab, 55 U.S.P.Q.2d 1313, 1318 (Fed. Cir. 2000) (emphasis added). Here again, there have been no such findings to establish that the features discussed above of the rejected claims are met by the reference relied upon. As referred to above, any review of the reference, whether taken alone or combined, makes plain that the reference simply does not describe the features discussed above of the rejected claims.

It is therefore respectfully submitted that claims 1, 10, and 13 are allowable for these reasons. Claims 2 to 4, 7, and 8 depend on claim 1, and are therefore allowable at least for the same reasons as claim 1. Claims 11 and 12 depend on claim 10, and are therefore allowable

at least for the same reasons as claim 10. Claims 14 depends on claim 13, and is therefore allowable at least for the same reasons as claim 13.

It is therefore respectfully submitted that the rejections of claims 1 to 4, 7, 8, and 10 to 14 should be withdrawn.

With respect to paragraph nine (9), claims 5 and 6 were rejected under 35 U.S.C. § 103(a) as unpatentable over the purported "admitted prior art" and the "Bengtsson" reference in view of U.S. Patent No. 6,697,972 ("Oshima").

Claims 5 and 6 depend from allowable claim 1. It is therefore respectfully requested that the obviousness rejections be withdrawn since claims 5 and 6 are allowable for essentially the same reasons as claim 1 as presented, and since the "Oshima" reference does not cure the critical deficiencies of the background information and the "Bengtsson" reference, which were explained above. This is because any review of the secondary "Oshima" reference makes clear that it simply does not in any way disclose or suggest the claim 1 features, as explained above. Accordingly, claims 5 and 6 are allowable.

With respect to paragraph ten (10), claim 9 was rejected under 35 U.S.C. § 103(a) as unpatentable over the purported "admitted prior art" and the "Bengtsson" reference in view of U.S. Patent No. 6,535,811 ("Rowland").

Claim 9 depends from allowable claim 1. It is therefore respectfully requested that the obviousness rejections be withdrawn since claim 9 is allowable for essentially the same reasons as claim 1, and since the secondary "Rowland" reference does not cure the critical deficiencies of the background information and the "Bengtsson" reference, which were explained above. This is because any review of the "Rowland" reference makes clear that it simply does not in any way disclose or suggest the claim 1 features, as explained above. Accordingly, claim 9 is allowable.

It is therefore respectfully submitted that claims 1 to 14 are allowable.

Conclusion

It is therefore respectfully submitted that all of claims 1 to 14 are allowable. It is therefore respectfully requested that the rejections be withdrawn, since all issues raised have been addressed and obviated. An early and favorable action on the merits is therefore respectfully requested.

Respectfully submitted,

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